Isolation Structures in Semiconductor Integrated Circuits (IC)
Background of the Invention

DESCRIPTION

[Para 1] 1. Technical Field

[Para 2] The present invention relates to semiconductor integrated circuits (IC), and more particularly, to isolation structures in semiconductor integrated circuits.

[Para 3] 2. Related Art

[Para 4] Typical isolation structures such as STI (Shallow Trench Isolation) structures, field oxide regions, etc., are used in a semiconductor integrated circuit (IC) to electrically isolate different devices (e.g., transistors, resistors, capacitors, etc.) formed on a same semiconductor substrate. The fabrication of such typical isolation structures involve multiple fabrication steps which can substantially add to the fabrication cost of the IC.

[Para 5] Therefore, there is a need for a novel isolation structure (and the method of forming the same) that requires simpler and fewer fabrication steps than that of the prior art.

[Para 6] Summary of the Invention

[Para 7] The present invention provides an isolation structure, comprising (a) a semiconductor substrate; and (b) an electric isolation region embedded in the semiconductor substrate, wherein the electric isolation region comprises (i) a bubble-implanted semiconductor region and (ii) an electrically insulating cap region on top of the bubble-implanted semiconductor region.

[Para 8] The present invention also provides a method for forming an isolation structure, the method comprising the steps of (a) providing a semiconductor substrate; (b) implanting gas bubbles into a semiconductor

region of the substrate so as to form a bubble-implanted semiconductor region in the substrate; and (c) forming an electrically insulating cap region on top of the bubble-implanted semiconductor region.

[Para 9] The present invention also provides a method for forming an isolation structure, the method comprising the steps of (a) providing a semiconductor substrate; (b) forming a hard mask layer on top of the semiconductor substrate; (c) creating an opening in the hard mask layer such that a top surface of the substrate is exposed to the atmosphere via the opening; (d) etching into the substrate via the opening; (e) implanting gas bubbles into a semiconductor region of the substrate via the opening so as to form a bubble-implanted semiconductor region in the substrate; and (f) forming an electrically insulating cap region on top of the bubble-implanted semiconductor region such that a top surface of the electrically insulating cap region is essentially at a same level as a top surface of the substrate.

[Para 10] The present invention provides a novel isolation structure (and the method of forming the same) that requires simpler and fewer fabrication steps than that of the prior art.

[Para 11] Brief Description of the Drawings

[Para 12] FIGs. 1A-1F show cross-section views of an isolation structure going through different fabrication steps, in accordance with embodiments of the present invention.

[Para 13] Detailed Description of the Invention

[Para 14] FIGs. 1A-1F show cross-section views of an isolation structure 100 going through different fabrication steps, in accordance with embodiments of the present invention. More specifically, with reference to FIG. 1A, in one embodiment, the fabrication process of the isolation structure 100 starts with the step of providing a semiconductor (silicon, germanium, etc.) substrate 110. Next, a pad oxide layer 120 is formed on top of the substrate 110. In one embodiment, the pad oxide layer 120 can be formed by thermally oxidizing a top surface 112 of the substrate 110.

[Para 15] Next, a nitride layer 130 is formed on top of the pad oxide layer 120. In one embodiment, the nitride layer 130 can be formed by CVD (Chemical Vapor Deposition) of silicon nitride on top of the pad oxide layer 120. The pad oxide layer 120 and the nitride layer 130 can be collectively referred to as the hard mask layer 120,130.

[Para 16] Next, with reference to FIG. 1B, in one embodiment, an opening 140 is created in the hard mask layer 120,130 by, illustratively, etching through the hard mask layer 120,130 until the top surface 112 of the substrate 110 is exposed to the atmosphere. In one embodiment, the step of etching through the hard mask layer 120,130 to form the opening 140 can involve photo-lithography and then dry etching.

[Para 17] Next, with reference to FIG. 1C, in one embodiment, the fabrication process of the isolation structure 100 further comprises the step of etching down into the substrate 110 to a surface 114. In one embodiment, the hard mask layer 120,130 can be used as a mask for the step of etching down into the substrate 110 via the opening 140. In one embodiment, the step of etching down into the substrate 110 via the opening 140 can involve dry etching. In one embodiment, the depth 116 of this surface 114 (with respect to the top surface 112 of the substrate 110) is such that an electrically insulating cap region 160 (FIG. 1E) which is later formed to a pre-specified thickness will have a top surface 162 at the same level as the top surface 112 of the substrate 110 as discussed *infra*.

[Para 18] Next, with reference to FIG. 1D, in one embodiment, a bubble-implanted semiconductor region 150 is formed in the substrate 110. In one embodiment, the bubble-implanted semiconductor region 150 can be formed in a gas implanting step (represented by an arrow 155, and hereafter referred to as the gas implanting step 155). In one embodiment, the gas implanting step 155 implants gas bubbles 152 into a region 150 of the substrate 110 so as to form the bubble-implanted semiconductor region 150. In one embodiment, the implanting gas used in the gas implanting step 155 can comprise a noble gas such as Argon, Xenon, etc. As a result, the gas bubbles

152 in the bubble-implanted semiconductor region 150 comprise the noble gas. The bubble-implanted semiconductor region 150 with the noble gas bubbles 152 would behave like a low-K material, wherein K is a dielectric constant. In one embodiment, the substrate 110 can comprise silicon. As a result, the bubble-implanted semiconductor region 150 comprises gas bubbles 152 surrounded by a silicon material.

[Para 19] In one embodiment, the gas implant step can have a range of implants rate of $5x10^{13}$ - $5x10^{17}$ atoms/cm^2 for different bubble sizes. In one embodiment, the implanting gas can comprise He, Ar, Ne, Xe, and/or H.

[Para 20] In one embodiment, range of implant energies depends upon the desired depth of the electric isolation region 150,160 (FIG. 1E) and the mass of the implant used. Typical ranges include 5 keV-30 keV for a material like He, but very shallow depths for the electric isolation region 150,160 (FIG. 1E) may require low energies like 100 eV. In contrast, very deep depths for the electric isolation region 150,160 (FIG. 1E) may require high energies like 50 keV. In one embodiment, an application may require a combination of low and high energies to cover shallow to deep depths for the electric isolation region 150,160 (FIG. 1E), respectively.

[Para 21] Next, in one embodiment, the structure 100 can be subjected to a heat cycle which causes the implanted gas bubbles 152 to merge and form larger gas bubbles 152. The heat cycle can be performed such that the average size of the resulting implanted gas bubbles 152 will reach a pre-specified average size after this heat cycle and other ensuing heat fabrication steps (e.g., thermal oxide heat cycles).

[Para 22] Next, with reference to FIG. 1E, in one embodiment, the electrically insulating cap region 160 is formed on top of the bubble-implanted semiconductor region 150. In one embodiment, if the bubble-implanted semiconductor region 150 comprises gas bubbles 152 surrounded by a silicon material, then the electrically insulating cap region 160 can be formed by thermally oxidizing a top surface 114 (FIG. 1D) of the bubble-implanted semiconductor region 150. As a result, a top surface 162 of the resulting

electrically insulating cap region 160 grows upward from the original surface 114 (FIG. 1D). The electrically insulating cap region 160 also expands downward from the original surface 114 to a bottom surface 117, which is also the new top surface 117 of the bubble-implanted semiconductor region 150. The resulting regions 150 and 160 can be collectively referred to as the electric isolation region 150,160.

[Para 23] In one embodiment, the depth 116 (FIG. 1C) is such that when the thickness 118 of the electrically insulating cap region 160 is grown to the pre-specified thickness, the top surface 162 of the electrically insulating cap region 160 is at the same level as the top surface 112 of the substrate 110.

[Para 24] Next, with reference to FIG. 1F, in one embodiment, the hard mask layer 120,130 (FIG. 1E) can be stripped off by, illustratively, wet etching. Alternatively, the hard mask layer 120,130 (FIG. 1E) can be stripped by chemical mechanical polishing (CVD). Then, in one embodiment, two transistors 170a and 170b can be formed on two opposing sides of the electric isolation region 150,160 in and at top of the substrate 110. As a result, the electric isolation region 150,160 can serve to electrically isolate the transistors 170a and 170b.

[Para 25] In summary, multiple isolation structures like the electric isolation region 150,160 can be formed in a same substrate to electrically isolate different devices (e.g., transistors, resistors, capacitors, etc.) of an IC. In one embodiment, the thickness 118 of the electrically insulating cap region 160 can be relatively small (100-300Å) compared with the thickness of an oxide layer of a typical STI layer which is usually 1,500Å thick. As a result, the formation of the electric isolation region 150,160 takes less time and therefore costs less than that of the prior art.

[Para 26] In addition, as a result of the top surface 162 of the electrically insulating cap region 160 being at the same level as the top surface 112 of the substrate 110, the resulting structure 100 of FIG. 1F has a planar top surface 112,116 which is beneficial for ensuing fabrication steps of forming devices and interconnect levels (not shown) in and on top of the substrate 110.

[Para 27] In one embodiment, with reference back to FIG. 1D, the implanting gas used for gas implanting step 155 can further comprise oxygen. As a result, the resulting gas bubbles 152 in the bubble-implanted semiconductor region 150 comprise oxygen. If the structure 100 is later heated (for instance, during the formation of the electrically insulating cap region 160 by thermal oxidation as shown in FIG. 1E), the oxygen in the gas bubbles 152 reacts with surrounding silicon material to form silicon dioxide at the edges of the gas bubbles 152. As a result, the gas bubbles 152 are now enclosed in silicon dioxide covers (not shown) and therefore essentially do not further increase in size when subjected to high temperatures.

[Para 28] While particular embodiments of the present invention have been described herein for purposes of illustration, many modifications and changes will become apparent to those skilled in the art. Accordingly, the appended claims are intended to encompass all such modifications and changes as fall within the true spirit and scope of this invention.